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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/776,009	02/02/2001	Michael A. Vyvoda	MA-027	7430

33971 7590 11/19/2003

MATRIX SEMICONDUCTOR, INC.
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EXAMINER	
MAI, ANH D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 11/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/776,009	VYVODA ET AL.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-14,30-34,36-48 and 50-62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-14,30-34,36-48 and 50-62* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Amendment

1. Amendment filed July 28, 2003 has been entered. Claims 6, 35 and 49 have been canceled. Claims 1, 30 and 44 have been amended. Claims 57-62 have been added. Claims 1-5, 7-14, 30-34, 36-48 and 50-62 are pending.

Claim Objections

2. Claims 1, 30 and 40 are objected to because of the following informalities:

Claim 1, lines 4, 5 and 7, respectively, recite: "the semiconductor regions" the correct term should be -- the polysilicon semiconductor regions --.

Claim 30, line 6, recites: "each of the regions" the correct term should be -- each of the polysilicon regions --.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-5, 7-14, 30-34, 36-48 and 50-62 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, lines 7-8 recites: "each of the [polysilicon] semiconductor regions have a shortest surface dimension that is less than or equal to **a first width**".

It is not known what is the width that "a first width" referring to.

Should the **first width** be the width of the wafer or the width of the semiconductor regions or the width of the dielectric regions ?

Claim Rejections - 35 USC § 102/103

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).
The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims **1**, 7, 8, 11, 12, 14, **30**, 36, 38, 39, 41, 43, **44**, 50, 51, 53, 54 and 6-62- are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Crafts et al. (U.S. Patent No. 5,920,110).

With respect to claims **1, 30** and **44**, insofar the device is concerned and as best understood by the examiner, Crafts teaches a wafer having a surface as claimed including:

a plurality of regions of dielectric (or means for attracting water, or hydrophilic material) (62) and polysilicon semiconductor (or means for repelling water, or hydrophobic material) (58) exposed at the surface of the wafer (52) the polysilicon semiconductor regions (58) formed over the wafer (52),

wherein the polysilicon semiconductor (58) regions have a total surface area that is less than or equal to a first fraction of a total surface area of the wafer (52) and

each of the polysilicon semiconductor regions (58) have a shortest surface dimension that is less than or equal to a first width,

the first fraction and the first width ensuring that the surface of the wafer can attract enough water to wet sufficiently allowing removal of residual particles therefrom. (See Figs. 6 and 7D).

Note that, in Fig. 7D, prior to the formation of layer (63) the surface of the polysilicon semiconductor regions (58) and dielectric region (62) are exposed.

Product by process limitation:

The expressions "after chemical mechanical planarization" and "allowing removal of residual particles therefrom" are taken to be a product by process limitation and is given no patentable weight. A product by process claim directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See *In re Fessman*, 180 USPQ 324, 326 (CCPA 1974); *In re Marosi et al.*, 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

With respect to the limitation "the polysilicon semiconductor regions have a total surface area that is less than or equal to a first fraction of a total surface area of the wafer", the polysilicon island (40, top view) has a total surface area (see Fig. 6), thus, the limitation of the claim is met.

With respect to the limitation "each of the polysilicon semiconductor regions have a shortest surface dimension that is less than or equal to a first width", since the polysilicon semiconductor region (58) of Crafts has a surface dimension and the "first width" is not defined, thus, the limitation of the claim is met.

With respect to the functional limitation: "the first fraction and the first width ensuring that the surface of the wafer can attract enough water to wet sufficiently allowing removal of residual particles therefrom", since the polysilicon semiconductor regions (58) have a total

surface area that is less than or equal to an unspecified first fraction, and the first width is undefined, thus, the wafer having a surface of Crafts should inherently function as claimed.

With respect to claims 7, 36 and 50, the dielectric regions or the means for attracting water or the hydrophilic material (62) of Crafts comprises silicon dioxide.

With respect to claims 8, 39 and 51, the regions of dielectric or the means for attracting water or the hydrophilic material (62) and polysilicon semiconductor or the means for repelling water or the hydrophobic material (58) of Crafts are alternate along the surface of the wafer (52).

With respect to claims 11, 38 and 53, the regions of dielectric or the means for attracting water or the hydrophilic material (62) of Crafts are rectangular. (See Fig. 6).

With respect to claims 12, 41 and 54, the regions of polysilicon semiconductor or the means for repelling water or the hydrophobic material (58) of Crafts are rectangular.

With respect to claims 14 and 56, the region of polysilicon semiconductor or the hydrophobic material (58) of Crafts are interspersed within a sea of dielectric (62). (See Fig. 6).

With respect to claim 43, the means for attracting (62) of Crafts comprises dielectric, the means for repelling (58) water comprises polysilicon semiconductor regions, and the semiconductor regions (58) are interspersed within a sea of dielectric (62).

With respect to claims 57, 59 and 61, the polysilicon semiconductor regions or the means for repelling water or polysilicon hydrophobic material (58) of Crafts comprises doped polysilicon.

With respect to claims 58, 60 and 62, the polysilicon semiconductor regions or the means for repelling water or polysilicon hydrophobic material (58) of Crafts comprises doped polysilicon.

Product by process limitation:

The expression "is doped by depositing a dopant along with polysilicon" is taken to be a product by process limitation and is given no patentable weight. A product by process claim directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See *In re Fessman*, 180 USPQ 324, 326 (CCPA 1974); *In re Marosi et al.*, 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not. In the instant case, the polysilicon semiconductor regions or the means for repelling water or polysilicon hydrophobic material (58) of Crafts comprises doped polysilicon. Thus, the limitation of the claims are met.

5. Claims **1**, 9, 10, **30**, 37, 40, **44** and 52 are further rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Liu et al. (U.S. Patent No. 5,612,914).

With respect to claims **1, 30** and **44**, insofar the device is concerned and as best understood by the examiner, Liu teaches a wafer having a surface as claimed including:

a plurality of regions of dielectric (or means for attracting water, or hydrophilic material) (50) and polysilicon semiconductor (or means for repelling water, or hydrophobic material) (30) exposed at the surface of the wafer (12) the polysilicon semiconductor regions (30) formed over the wafer (12),

wherein the polysilicon semiconductor (30) regions have a total surface area that is less than or equal to a first fraction of a total surface area of the wafer (12) and

each of the polysilicon semiconductor regions (30) have a shortest surface dimension that is less than or equal to a first width,

the first fraction and the first width ensuring that the surface of the wafer can attract enough water to wet sufficiently allowing removal of residual particles therefrom. (See Figs. 4a and 4ccol. 6, ll. 1-43).

With respect to: the first width, the first fraction, the sufficiently wet and *Product-by-process limitation*, a similar reasoning as that of claim 1 is also applied here.

With respect to claims 9 and 37, the regions of dielectric (or the means for attracting water) (50) of Liu are elongated strips. (See Fig. 4c).

With respect to claims10 and 40, the polysilicon semiconductor or the means for repelling water (30) of Liu are elongated strips of semiconductor. (See Fig. 4c).

With respect to claim 52, the regions of hydrophilic material (50) and hydrophobic material (30) of Liu are elongated strips. (See Fig. 4c).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 2-5, 31-34 and 45-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Crafts '110.

With respect to claims 2, 31 and 45; 3, 32 and 46, Crafts teaches the polysilicon semiconductor regions (58) have a total surface are that is less than equal to a first fraction of the total surface area of the wafer (52). (See Figs. 6 and 7D).

Thus, Crafts is shown to teach all the features of the claim with the exception of explicitly disclosing the first fraction to be 50 % or 60 % of the total surface area of the wafer. The claimed fractions do not appear to be critical.

Note that the specification contains no disclosure of either the *critical nature of the claimed first fractions of any unexpected results arising therefrom.* Where patentability is aid to based upon particular chosen dimension or upon another variable recited in a claim, the Applicant must show that the chosen dimension are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Although Crafts does not explicitly disclosing a fraction of 50 % or 60 %, however, from Figs 6 and 7D, one having ordinary skill in the art would have concluded that the polysilicon semiconductor regions (58) (shown as islands 40, within the dielectric region 62, blank area, in fig. 6) have a total surface area which is less than 50 % of the total surface area of the wafer (52).

With respect to claims 4, 33 and 47; 5, 34 and 48, Crafts teaches each of the polysilicon semiconductor regions (58) have a shortest surface dimension that is less than or equal to a first width (?). (See Figs. 1, 3, 6 and 7D).

Thus, Crafts is shown to teach all the features of the claim with the exception of explicitly disclosing dimension of the first width. The claimed dimensions (500 microns or 2.5 millimeters) of the first width do not appear to be critical.

Note that the specification contains no disclosure of either the *critical nature of the claimed dimension of the first width of any unexpected results arising therefrom.* Where patentability is aid to based upon particular chosen dimension or upon another variable recited in a claim, the Applicant must show that the chosen dimension are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Although Crafts does not explicitly disclosing a dimension of the first width (?), however, from Figs 1, 3, 6 and 7D and col. 3. lines 4-12, one having ordinary skill in the art would have concluded that each of the polysilicon semiconductor regions (58) should have a shortest surface dimension that is less than the first width of 500 microns or 2.5 millimeters because between 25,000 to 50,000 gates (or more) only occupied an area of 10 millimeters square, therefore, the shortest surface dimension of each of the polysilicon semiconductor regions (58) should definitely less than 500 microns or 2.5 millimeters.

7. Claims 13, 42 and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee '696 as applied to claims 1, 30 and 44 above, and further in view of Inoue (U.S. Patent No. 4,656,054) of record.

Crafts teaches that the polysilicon semiconductor regions (58) having rectangular shape.

Thus, Crafts is shown to teach all the features of the claim with the exception of form the polysilicon semiconductor regions (58) having an alternate shape such as of hexagon.

However, Inoue teaches semiconductor regions can be formed in to various shapes using a mask having various shapes including hexagon. (See Fig. 8).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the polysilicon semiconductor region of Crafts having hexagonal shapes as taught by Inoue because more polysilicon semiconductor island having hexagonal shape can be made in a given area (Fig. 8) than the other shapes. (See Figs. 5 and 6).

Response to Arguments

8. Applicant's arguments with respect to all claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (703) 305-0575. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

A.M
November 17, 2003